Electronic Version
Stylesheet Version v1.1.1

# Claims

[c1] Method of forming a transistor comprising:
disposing a planar platform of silicon atop a support structure of oxide which is atop a substrate;
forming gate structures both atop and beneath the planar platform; and
forming source and drain diffusions within the planar platform.

[c2] Method, according to claim 1, wherein:
the gate structures which are formed beneath the planar platform are smaller than the planar platform.

[c3] Method, according to claim 1, wherein:
the gate structures which are formed beneath the planar platform are aligned with the gate structures which are formed atop the planar platform.

[c4] Transistor, comprising:
a substrate,
a standoff structure of oxide formed atop the substrate;
a planar pedestal of silicon formed atop the standoff structure;
at least one top gate electrode formed on the planar

pedestal; and
source and drain diffusions formed in the planar pedestal.

[c5] Transistor, according to claim 4, further comprising:
a back gate electrode formed under the planar pedestal.

[c6] Transistor, according to claim 4, wherein:
the back gate electrode has a length and width approximately equal to a length and width of the planar pedestal.

[c7] Transistor, according to claim 4, wherein:
the back gate electrode wraps around side edges of the planar pedestal.

[c8] Transistor, according to claim 4, wherein:
the back gate electrode is smaller than the planar pedestal.

[c9] Transistor, according to claim 4, wherein:
there are two top gates; and
the back gate electrode is aligned under the two top gates.

[c10] Transistor, according to claim 4, wherein:
there are two top gates; and
inner edges of the top gates are aligned with outer edges

of the standoff structure.

[c11] Method of forming a transistor comprising:
providing an SOI wafer comprising a handle substrate, a buried oxide layer (BOX) disposed atop the handle substrate and a silicon-on-insulator (SOI) layer disposed atop the buried oxide layer;
in a first etching step, patterning the SOI layer to become the active silicon layer of an SOI transistor, wherein a portion of the buried oxide layer is underneath the patterned SOI layer and other portions of the buried oxide layer are not underneath the patterned silicon layer, and wherein a top surface of the SOI layer is exposed;
in a second etching step, etching the portions of the buried oxide layer which are not underneath the patterned silicon layer, thereby exposing a portion of a top surface of the handle substrate;
in a third etching step, removing the buried oxide layer from under the patterned silicon layer to form a standoff structure, thereby exposing a portion of a bottom surface of the SOI layer;
performing gate oxidation, thereby forming gate oxide on the exposed surfaces of the patterned silicon layer;
depositing gate electrode material atop the handle substrate and covering the standoff structure as well as the patterned SOI layer; and

in a fourth etching step, etching the gate electrode material to form at least one gate stack atop the SOI layer.

[c12] Method, according to claim 11, further comprising:
in a fifth etching step, etching the gate electrode material to form a back gate beneath the SOI layer.

[c13] 13.Method, according to claim 11, wherein:
the back gate is aligned with the at least one gate stack.

[c14] Method, according to claim 11, wherein:
the third etching step exposes a substantial portion of the underside of the patterned silicon layer.

[c15] Method, according to claim 11, wherein:
the third etching step exposes approximately 80% of the underside of the patterned silicon layer.

[c16] Method, according to claim 11, wherein:
the third etching step exposes additional portions of the handle substrate.

[c17] Method, according to claim 11, wherein:
during gate oxidation, gate oxide is also formed on the exposed surface of the handle substrate.

[c18] Method, according to claim 11, further comprising:
prior to the fourth etching step, depositing a hard mask material on top of the gate electrode material;

defining the hard mask material;
then performing the fourth etching step;
then removing the hard mask.

[c19] Method, according to claim 11, wherein:
the gate stack is etched in the fourth etching step using an anisotropic dry etch that is selective to the gate oxide.

[c20] Method, according to claim 11, wherein:
in the fourth etching step, the gate electrode material is etched down to approximately the level of the top surface of the SOI layer, thereby creating electrode structures atop the SOI layer and isolated therefrom by gate oxide.